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Jay H Maioli
Cooper & Dunham
1185 Avenue of the Americas
New York, NY 10036

EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/744,279	SAKAMOTO, ICHIRO	
	Examiner	Art Unit	
	Jason E Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Applicant's amendment filed on 8/24/04. The amendment includes amendments to the disclosure as well as amendments to the claims. Claims 1-20 are currently pending in the application.

Specification

2. The previous objections to the disclosure are withdrawn due to the Applicant's amendments.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 5, 7, 11, 15, and 17 all contain the limitation "the second digital signal processing apparatus transmits the data via the predetermined digital bus". It is unclear from the claims what data the phrase "the data" is referring to. For example, both "real-time data" and "asynchronous data" are described in

each of these claims. It is recommended that these claims be amended to more clearly state which data is meant by the phrase "the data".

Claims 2-4, 6, 8-10, 12-14, 16, and 18-20 are also rejected since they each depend on one of the above rejected claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3-5, 7, 9-11, 13-15, 17, and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rosefield et al. (U.S. Pat. 5986589).

With respect to claims 1 and 11, Rosefield et al. discloses a digital signal processing system and method including a first digital signal processing apparatus, digital signal processor 34, connected via a predetermined digital bus to a second digital signal processing apparatus, sample rate converter 36 **(See column 3 line 53 to column 4 line 3 and items 34 and 36 in Figure 1 of Rosefield et al. for reference to digital signal processor 34, which is a first digital signal processing apparatus, and sample rate converter 36, which is**

a second digital signal processing apparatus, being connected via a PCI Bus and also connected via directly to each other as shown in Figure 1). Rosefield et al. also discloses that the second digital signal processing apparatus, sample rate converter 36, has a data transmission rate that can be controlled by other apparatuses on the digital bus **(See column 3 line 53 to column 4 line 29 of Rosefield et al. for reference to the sample rate converter 36 using data sent from the DSP 34, which is an other apparatus on the digital bus, to externally control the data rate that data sent to the sample rate converter will be transmitted at).** Rose field et al. further discloses the digital signal processor 34 having a generating means for generating a command for making an inquiry to the second digital signal processing apparatus, sample rate converter 36, connected via the digital bus about a capability of rate control functions of the unit and a transmitting means for transmitting the command via the predetermined transmission line **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to DSP 34 generating and control logic reset message in step 130, which is a command inquiry about rate control functions, and sending it to the sample rate converter 36, meaning that there must be a means in the DSP for generating and transmitting the control logic reset message).** Rosefield et al. also discloses a receiving means for receiving a response to the transmitted command **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to the DSP 34 receiving an interrupt trigger in step 138, which is a response sent from the sample rate converter 36 to the control logic**

reset message in step 130). Rosefield et al. further discloses that the predetermined digital bus supports real-time data transmission for transmitting audio data and asynchronous data transmission for transmitting control data **(See column 1 line 25-47 and column 4 lines 8-29 of Rosefield et al. for reference to the system converting the data rate of real time audio sent from audio devices over a bus and for reference to command data, which is asynchronous, also being sent over the bus)**. Rosefield et al. also discloses that the second digital signal processing apparatus transmits the data via the predetermined digital bus **(See column 4 lines 8-29 and Figure 2 of Rosefield et al. for reference to the sample rate converter receiving data from the DSP 36 though the direct bus connection between the devices)**.

With respect to claims 3 and 13, Rosefield et al. discloses a recognizing means for recognizing, based on the received response, the rate control functions of the second digital signal processing apparatus **(See column 7 lines 1-63 and Figure 5 of Rosefield et al. for reference to the interrupt trigger sent in step 138 from the sample rate converter 36 to the DSP 34 being a signal that tells the DSP 34 that the sample rate converter 36 is ready for the rate control information to be sent to it)**.

With respect to claims 4 and 14, Rosefield et al. discloses a control means and method in the digital signal processor 34 for controlling the transmission rate in accordance with the rate control of the second digital signal processing apparatus recognized based on the received response **(See column 7 lines 1-16, column 4 line 59 to column 5 line 12 and Figures 3 and 5 of**

Rosefield et al. for reference to the DSP 34 generating variable rate control data 50 and sending this variable rate control data to sample rate converter 36, with the rate control data 50 indicating the rate that the data should be transmitted at in the sample rate converter 36).

With respect to claims 5 and 15, Rosefield et al discloses a digital signal processing system and method including a first digital signal processing apparatus, DSP 34, connected via a predetermined digital bus to a second digital signal processing apparatus, sample rate converter 36 **(See column 3 line 53 to column 4 line 3 and items 34 and 36 in Figure 1 of Rosefield et al. for reference to digital signal processor 34, which is a first digital signal processing apparatus, and sample rate converter 36, which is a second digital signal processing apparatus, being connected via a PCI Bus and also connected via directly to each other as shown in Figure 1)**. Rosefield et al. also discloses that the second digital signal processing apparatus, sample rate converter 36, has a data transmission rate that can controlled by other apparatuses on the digital bus **(See column 3 line 53 to column 4 line 29 of Rosefield et al. for reference to the sample rate converter 36 using data sent from the DSP 34, which is an other apparatus on the digital bus, to externally control the data rate that data sent to the sample rate converter will be transmitted at)**. Rosefield et al. further discloses the sample rate converter 36 including a receiving means for receiving a command for inquiry of a rate control transmitted from the unit, DSP 34, via the predetermined transmission line **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield**

et al. for reference to DSP 34 generating and control logic reset message in step 130, which is a command, and sending it to the sample rate converter 36, meaning that there must be a means in the sample rate converter 36 for receiving the control logic reset message). Rosefield et al. also discloses an examining means for examining, based on the command, the rate control of the digital signal processor, sample rate converter 36 **(See column 7 lines 1-16 and Figure 5 of Rosefield et al. for reference to the sample rate converter 36 determining, or examining, if an interrupt retrigger has been sent in step 136)**. Rosefield et al. further discloses a sending means for sending back a result of the examination **(See column 7 lines 1-16 and Figure 5 of Rosefield et al. for reference to the sample rate converter 36 sending back an interrupt to the DSP 34 in step 138 as a result of the examination in step 136)**. Rosefield et al. further discloses that the predetermined digital bus supports real-time data transmission for transmitting audio data and asynchronous data transmission for transmitting control data **(See column 1 line 25-47 and column 4 lines 8-29 of Rosefield et al. for reference to the system converting the data rate of real time audio sent from audio devices over a bus and for reference to command data, which is asynchronous, also being sent over the bus)**. Rosefield et al. also discloses that the second digital signal processing apparatus transmits the data via the predetermined digital bus **(See column 4 lines 8-29 and Figure 2 of Rosefield et al. for reference to the sample rate converter receiving data from the DSP 36 though the direct bus connection between the devices)**.

With respect to claims 7 and 17, Rosefield et al. discloses a system and method with a first digital signal processing apparatus, digital signal processor 34, connected via a predetermined digital bus to a second digital signal processing apparatus, sample rate converter 36 **(See column 3 line 53 to column 4 line 3 and items 34 and 36 in Figure 1 of Rosefield et al. for reference to digital signal processor 34, which is a first digital signal processing apparatus, and sample rate converter 36, which is a second digital signal processing apparatus, being connected via a PCI Bus and also connected via directly to each other as shown in Figure 1)**. Rosefield et al. also discloses that the second digital signal processing apparatus, sample rate converter 36, has a data transmission rate that can controlled by other apparatuses on the digital bus **(See column 3 line 53 to column 4 line 29 of Rosefield et al. for reference to the sample rate converter 36 using data sent from the DSP 34, which is an other apparatus on the digital bus, to externally control the data rate that data sent to the sample rate converter will be transmitted at)**. Rosefield et al. further discloses the digital signal processor 34 having a generating means for generating a command for making an inquiry to the second digital signal processing apparatus, sample rate converter 36, connected via the predetermined digital bus about a capability of rate control functions of the second digital signal processing apparatus and a transmitting means for transmitting the command via the predetermined digital bus **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to DSP 34 generating and control logic reset message in step**

130, which is a command inquiry about rate control functions, and sending it to the sample rate converter 36, meaning that there must be a means in the DSP for generating and transmitting the control logic reset message). Rosefield et al. also discloses a first receiving means for receiving a response to the transmitted command **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to the DSP 34 receiving an interrupt trigger in step 138, which is a response sent from the sample rate converter 36 to the control logic reset message in step 130).** Rosefield et al. further discloses the sample rate converter 36 including a second receiving means for receiving a command for making an inquiry about a capability of rate control functions transmitted from the second digital signal processing apparatus via the predetermined digital bus **(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to DSP 34 generating and control logic reset message in step 130, which is a command, and sending it to the sample rate converter 36, meaning that there must be a means in the sample rate converter 36 for receiving the control logic reset message).** Rosefield et al. also discloses an examining means for examining, based on the command, the rate control functions of the digital signal processor, sample rate converter 36 **(See column 7 lines 1-16 and Figure 5 of Rosefield et al. for reference to the sample rate converter 36 determining, or examining, if an interrupt retrigger has been sent in step 136).** Rosefield et al. further discloses a sending means for sending back a result of the examination **(See column 7 lines 1-16 and Figure 5 of Rosefield et al. for reference to the sample rate converter 36**

sending back an interrupt to the DSP 34 in step 138 as a result of the examination in step 136). Rosefield et al. further discloses that the predetermined digital bus supports real-time data transmission for transmitting audio data and asynchronous data transmission for transmitting control data **(See column 1 line 25-47 and column 4 lines 8-29 of Rosefield et al. for reference to the system converting the data rate of real time audio sent from audio devices over a bus and for reference to command data, which is asynchronous, also being sent over the bus)**. Rosefield et al. also discloses that the second digital signal processing apparatus transmits the data via the predetermined digital bus **(See column 4 lines 8-29 and Figure 2 of Rosefield et al. for reference to the sample rate converter receiving data from the DSP 36 though the direct bus connection between the devices)**.

With respect to claims 9 and 19, Rosefield et al. discloses a recognizing means for recognizing the rate control functions of the second digital signal processing apparatus based on the received response **(See column 7 lines 1-63 and Figure 5 of Rosefield et al. for reference to the interrupt trigger sent in step 138 from the sample rate converter 36 to the DSP 34 being a signal that tells the DSP 34 that the sample rate converter 36 is ready for the rate control information to be sent to it)**.

With respect to claims 10 and 20, Rosefield et al. discloses a control means and method in the digital signal processor 34 for controlling the transmission rate in accordance with the rate control function of the second digital signal processing apparatus recognized based on the received response

(See column 7 lines 1-16, column 4 line 59 to column 5 line 12 and Figures 3 and 5 of Rosefield et al. for reference to the DSP 34 generating variable rate control data 50 and sending this variable rate control data to sample rate converter 36, with the rate control data 50 indicating the rate that the data should be transmitted at in the sample rate converter 36).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 6, 8, 12, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosefield et al. in view of Lin (U.S. Pat. 5907295).

With respect to claims 2, 6, 8, 12, 16, and 18, Rosefield et al. discloses the rate control of the second digital signal processing apparatus, sample rate converter 36, including a base data transmission rate control **(See column 4 line 8 to column 5 line 12 of Rosefield et al. for reference to DSP 34 controlling the base rate of the data being converted and transmitted from sample rate converter 36)**. Rosefield et al. does not disclose a synchronous control and a variable rate control for fine adjustment of a base data transmission rate.

Lin, in the field of communications, discloses a audio sample-rate conversion system and method that uses a synchronous control and a variable rate control for fine adjustment of a base data transmission rate **(See column 3 line 65 to column 4 line 4 of Lin for reference to using a coarse sample-rate adjustment, which is a synchronous control, and a fine adjustment, which is a variable rate control for fine adjustment of a base data transmission rate)**. Using a synchronous control and a variable rate control for fine adjustment of a base transmission rate has the advantage of allowing greater control over the exact transmission rate of data by allowing the rate to be adjusted in small increments.

It would have been obvious to one of ordinary skill in the art at the time of the invention, when presented with the work of Lin, to combine the use of a synchronous control and a variable rate control for fine adjustment of a base transmission rate, as suggested by Lin, with the system and method of Rosefield et al., with the motivation being to allow greater control over the exact transmission rate of data by allowing the rate to be adjusted in small increments.

Response to Arguments

9. Applicant's arguments filed on 8/24/04 have been fully considered but they are not persuasive.

In response to Applicant's argument that:

> "neither the cited section nor the remainder of Rosefield et al. disclose a first digital signal processing apparatus connected via a digital bus to a second digital signal processing apparatus whose data transmission rate can be controlled by other apparatuses on the digital bus"

the Examiner respectfully disagrees. As discussed in the rejections above, Rosefield et al. does disclose a DSP 36, which is a first digital signal processing apparatus, connected though a bus to a sample rate converter 34, which is a second digital signal processing apparatus, with the data transmission rate of the sample rate converter being controlled by the DSP 36.

In response to Applicant's argument that:

> "Additionally, it is submitted that Rosefield et al. does not disclose generating means for generating a command for making an inquiry to the second digital signal processing apparatus about a capability of rate control functions, and that the predetermined digital bus supports real-time data transmission for transmitting audio/visual data and asynchronous control data"

the Examiner respectfully disagrees. As discussed in the rejections above, Rosefield et al. discloses the digital signal processor 34 having a generating means for generating a command for making an inquiry to the second digital signal processing apparatus, sample rate converter 36, connected via the digital bus about a capability of rate control functions of the unit and a transmitting means for transmitting the command via the predetermined transmission line

(See column 7 lines 1-16 and Figures 3 and 5 of Rosefield et al. for reference to DSP 34 generating and control logic reset message in step 130, which is a command inquiry about rate control functions, and sending it to the sample rate converter 36, meaning that there must be a means in the DSP for generating and transmitting the control logic reset message). Also, as discussed in the rejections above, Rosefield et al. discloses that the predetermined digital bus supports real-time data transmission for transmitting audio data and asynchronous data transmission for transmitting control data **(See column 1 line 25-47 and column 4 lines 8-29 of Rosefield et al. for reference to the system converting the data rate of real time audio sent from audio devices over a bus and for reference to command data, which is asynchronous, also being sent over the bus).**

In response to Applicant's argument that:

> "it is respectfully submitted that there is no motivation within the cited references to combine the elements in the manner suggested in the Office Action"

the Examiner reminds the applicant that the motivation to combine references in a 35 USC § 103 rejection does not necessarily have to be found within the references themselves. Section 706.02(j) of the MPEP states:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves **or in the knowledge generally**

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings."

The highlighted section shows that the motivation to combine does not need to be found in the references themselves.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jem

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600